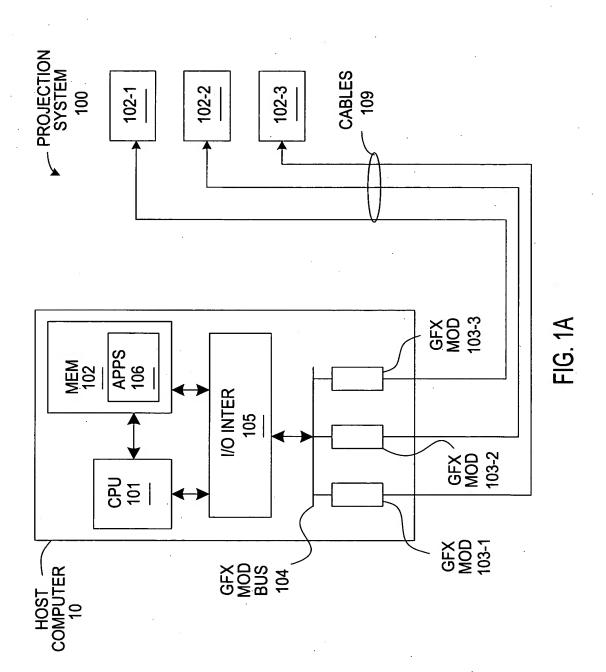ATTY DKT. NO.: NVDA/P000876
U.S. SERIAL NO.: UNKNOWN
FILED: HEREWITH
APPLICANT: NVIDIA Corporation
TITLE: METHOD FOR TESTING SYNCHRONIZATION AND CONNECTION
STATUS OF A GRAPHICS PROCESSING UNIT MODULE
INVENTOR: IAN M. WILLIAMS, ET AL.
EXPRESS MAIL NO.: EV335471017US   PAGE 1 OF 27

FIG. 1A

ATTY DKT. NO.: NVDA/P000876
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APPLICANT: NVIDIA Corporation
TITLE: METHOD FOR TESTING SYNCHRONIZATION AND CONNECTION
STATUS OF A GRAPHICS PROCESSING UNIT MODULE
INVENTOR: IAN M. WILLIAMS, ET AL.
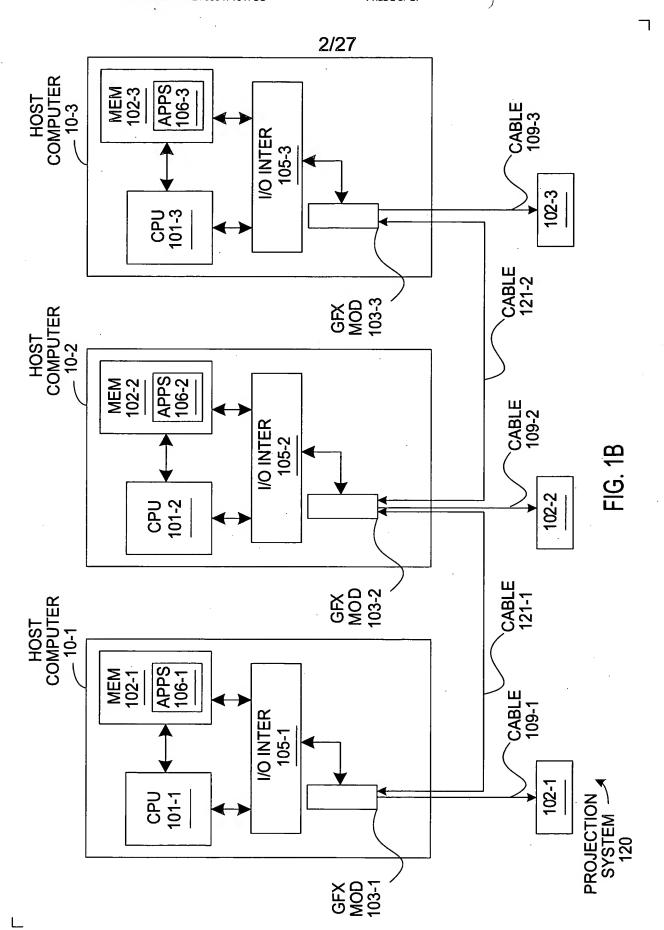EXPRESS MAIL NO.: EV335471017US   PAGE 2 OF 27

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FIG. 1B

ATTY DKT. No.: NVDA/P000876
U.S. SERIAL No.: UNKNOWN
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APPLICANT: NVIDIA Corporation
TITLE: METHOD FOR TESTING SYNCHRONIZATION AND CONNECTION
STATUS OF A GRAPHICS PROCESSING UNIT MODULE
INVENTOR: IAN M. WILLIAMS, ET AL.
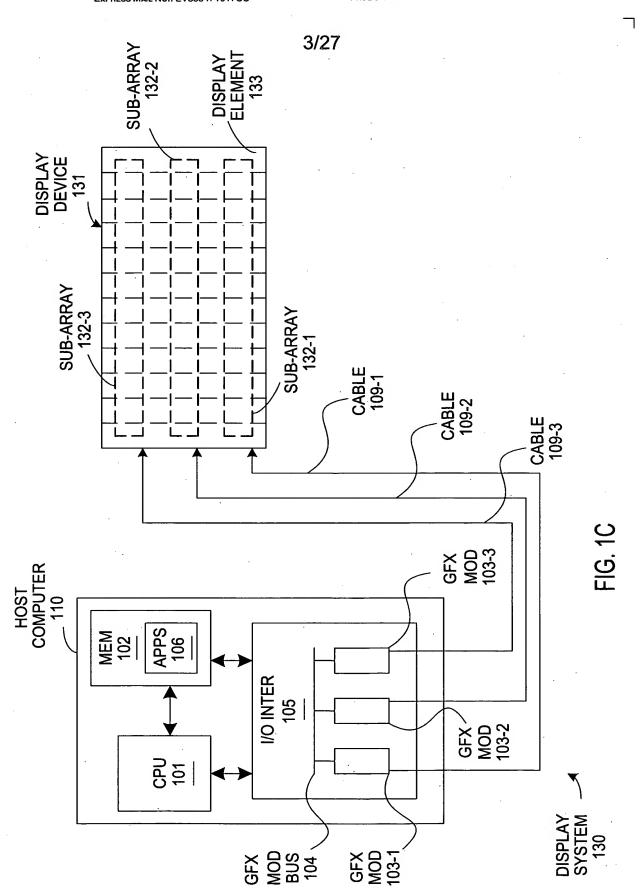EXPRESS MAIL No.: EV335471017US   PAGE 3 OF 27

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FIG. 1C

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APPLICANT: NVIDIA Corporation
TITLE: METHOD FOR TESTING SYNCHRONIZATION AND CONNECTION
STATUS OF A GRAPHICS PROCESSING UNIT MODULE
INVENTOR: IAN M. WILLIAMS, ET AL.
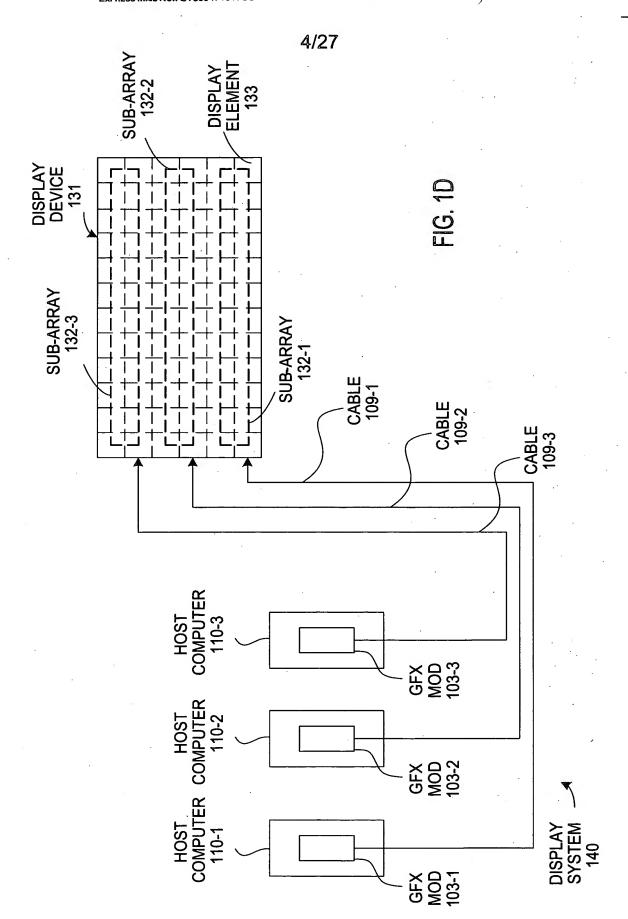EXPRESS MAIL NO.: EV335471017US   PAGE 4 OF 27

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FIG. 1D

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TITLE: METHOD FOR TESTING SYNCHRONIZATION AND CONNECTION
STATUS OF A GRAPHICS PROCESSING UNIT MODULE
INVENTOR: IAN M. WILLIAMS, ET AL.
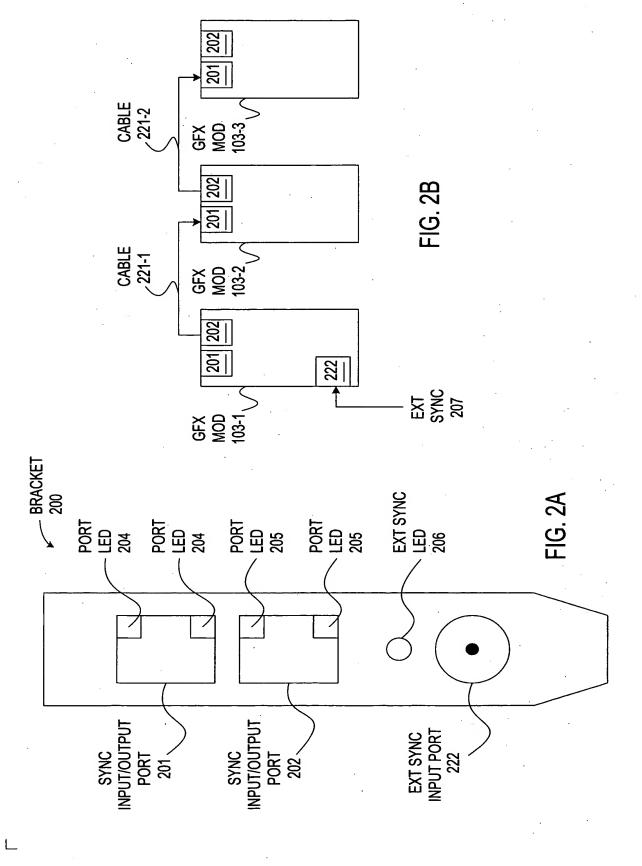EXPRESS MAIL NO.: EV335471017US   PAGE 5 OF 27

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FIG. 2B

FIG. 2A

ATTY DKT. NO.: NVDA/P000876
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STATUS OF A GRAPHICS PROCESSING UNIT MODULE
INVENTOR: IAN M. WILLIAMS, ET AL.
EXPRESS MAIL NO.: EV335471017US   PAGE 6 OF 27
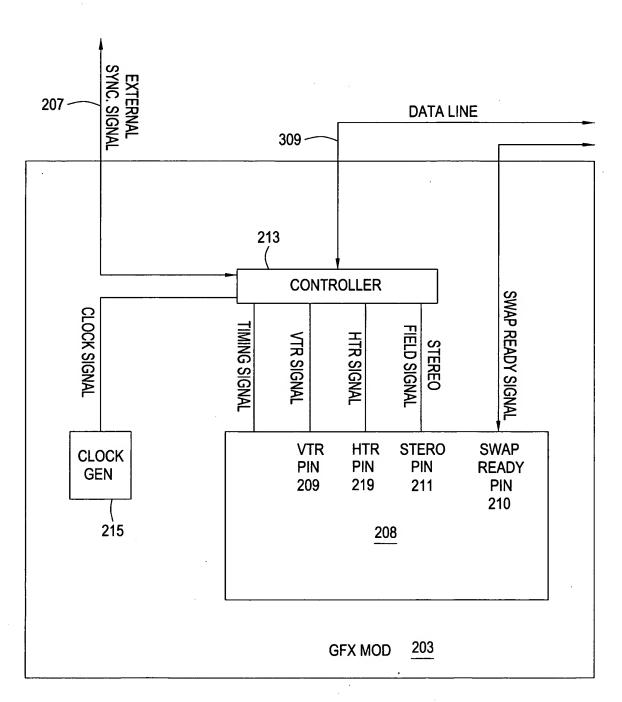
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FIG. 2C

Atty Dkt. No.: NVDA/P000876
U.S. Serial No.: UNKNOWN
Filed: HEREWITH
Applicant: NVIDIA Corporation
Title: Method For Testing Synchronization and Connection
Status of A Graphics Processing Unit Module
Inventor: Ian M. Williams, et al.
Express Mail No.: EV335471017US   Page 7 of 27

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FIG. 2D

ATTY DKT. NO.: NVDA/P000876
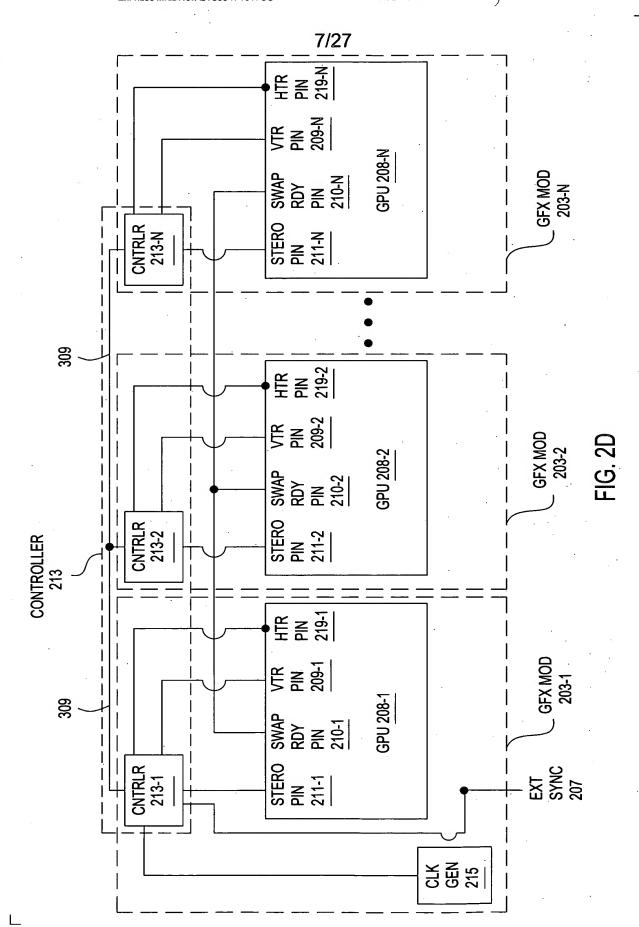U.S. SERIAL NO.: UNKNOWN
FILED: HEREWITH
APPLICANT: NVIDIA CORPORATION
TITLE: METHOD FOR TESTING SYNCHRONIZATION AND CONNECTION
STATUS OF A GRAPHICS PROCESSING UNIT MODULE
INVENTOR: IAN M. WILLIAMS, ET AL.
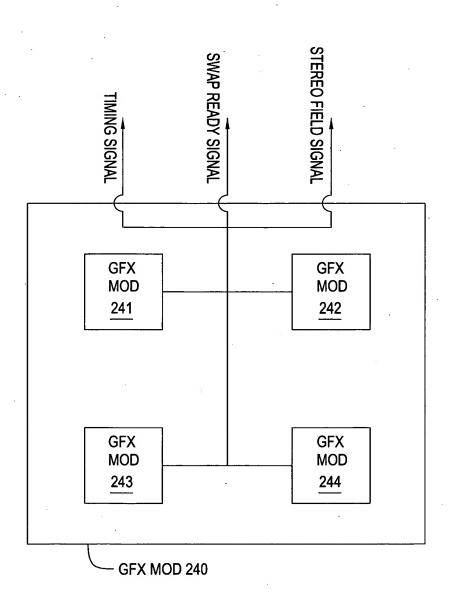EXPRESS MAIL NO.: EV335471017US   PAGE 8 OF 27

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TIMING SIGNAL

SWAP READY SIGNAL

STEREO FIELD SIGNAL

GFX
MOD
241

GFX
MOD
242

GFX
MOD
243

GFX
MOD
244

GFX MOD 240

FIG. 2E

Atty Dkt. No.:	NVDA/P000876
U.S. Serial No.:	UNKNOWN
Filed:	HEREWITH
Applicant:	NVIDIA Corporation
Title:	Method For Testing Synchronization and Connection Status of A Graphics Processing Unit Module
Inventor:	Ian M. Williams, ET AL.
Express Mail No.: EV335471017US	Page 9 of 27

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FIG. 3

ATTY DKT. NO.:   NVDA/P000876
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APPLICANT: NVIDIA CORPORATION
TITLE: METHOD FOR TESTING SYNCHRONIZATION AND CONNECTION
                        STATUS OF A GRAPHICS PROCESSING UNIT MODULE
INVENTOR: IAN M. WILLIAMS, ET AL.
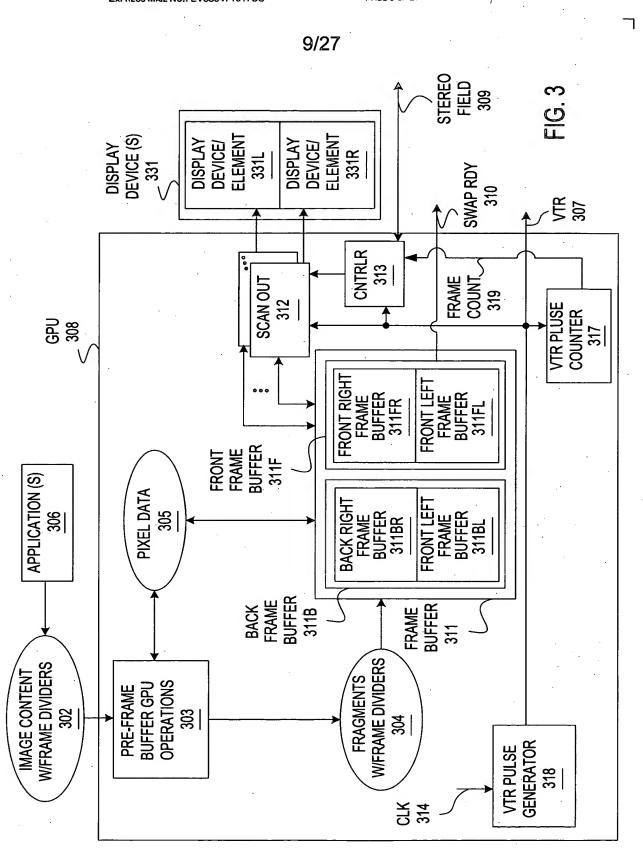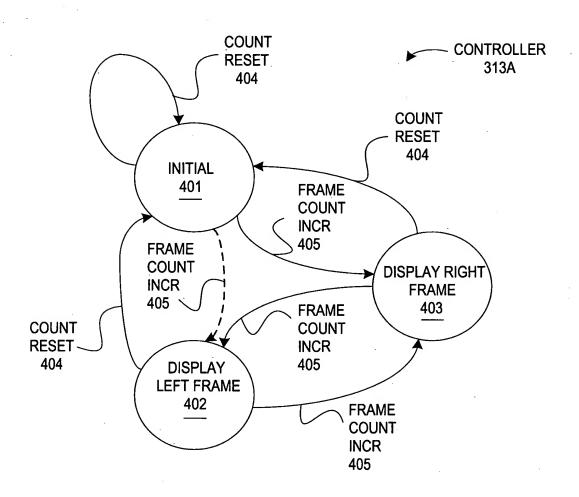EXPRESS MAIL NO.: EV335471017US   PAGE 10 OF 27

FIG. 4A

FIG. 4B

FIG. 4D

ATTY DKT. No.: NVDA/P000876
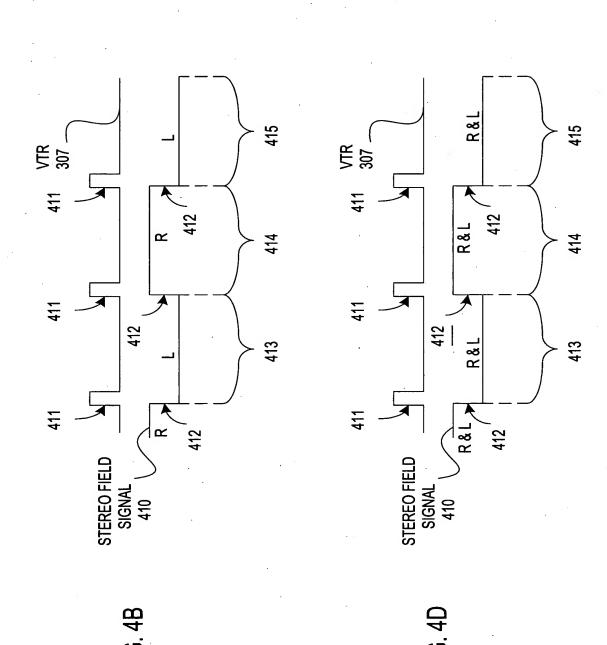U.S. SERIAL No.: UNKNOWN
FILED: HEREWITH
APPLICANT: NVIDIA Corporation
TITLE: METHOD FOR TESTING SYNCHRONIZATION AND CONNECTION
STATUS OF A GRAPHICS PROCESSING UNIT MODULE
INVENTOR: IAN M. WILLIAMS, ET AL.
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FIG. 4C

440

442

CLOCK
SIGNAL IN PHASE
WITH EXT. SYNC
SIGNAL ?

NO

444

ADJUST FREQUENCY
OF CLOCK GENERATOR

YES

TRANSMIT TIMING SIGNAL
TO GPU'S

446

FIG. 4E

452 — **IS PHASE OF TIMING SIGNAL FROM MASTER GPU IN SYNC. WITH PHASE OF TIMING SIGNAL FROM SLAVE GRAPHICS MODULE ?**

NO → 454 **ADJUST FREQUENCY OF CLOCK GENERATOR OF SLAVE GRAPHICS MODULE**

YES

456 — **IS PHASE OF STEREO FIELD SIGNAL OF MASTER GRAPHICS MODULE IN SYNC. WITH PHASE OF STEREO FIELD SIGNAL OF SLAVE GRAPHICS MODULE ?**

NO → 458 **ADJUST STEREO FIELD PHASE OF SLAVE GRAPHICS MODULE**

YES

460 **TRANSMIT TIMING SIGNAL AND STEREO FIELD SIGNAL FROM MASTER GRAPHICS MODULE TO OTHER SLAVE GRAPHICS MODULE**

FIG. 4F

Atty Dkt. No.: NVDA/P000876
U.S. Serial No.: UNKNOWN
Filed: HEREWITH
Applicant: NVIDIA Corporation
Title: Method For Testing Synchronization and Connection
Status Of A Graphics Processing Unit Module
Inventor: Ian M. Williams, ET AL.
Express Mail No.: EV335471017US   Page 15 of 27
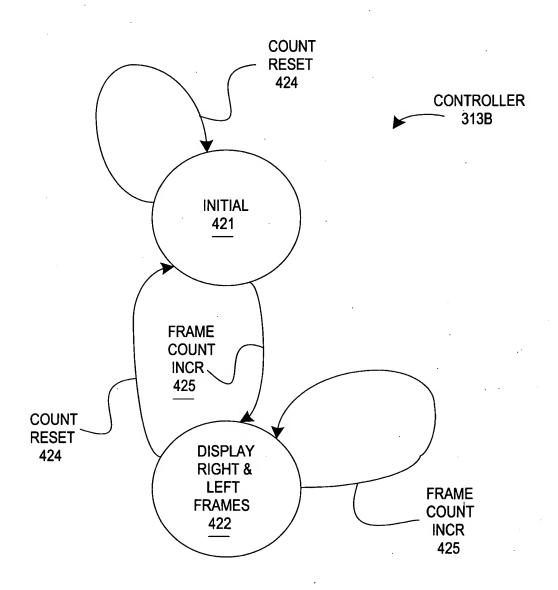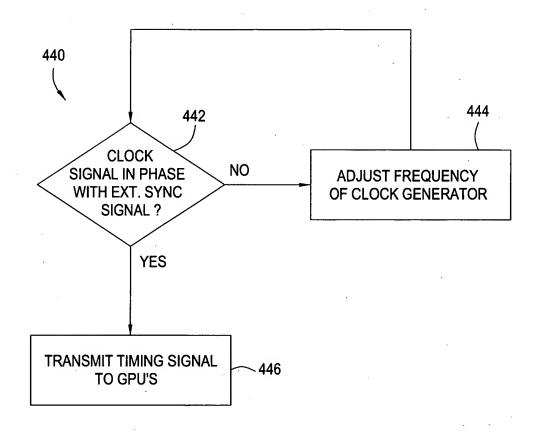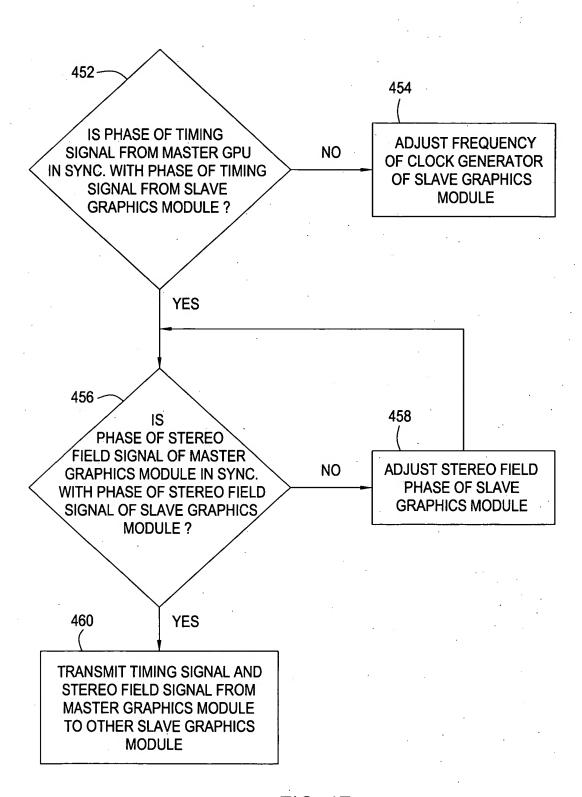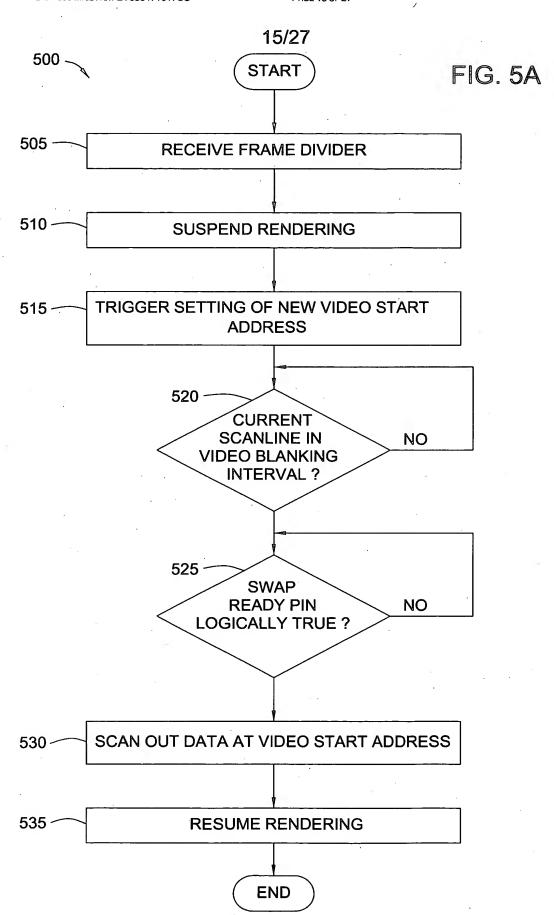
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FIG. 5A

500

START

505 — RECEIVE FRAME DIVIDER

510 — SUSPEND RENDERING

515 — TRIGGER SETTING OF NEW VIDEO START ADDRESS

520 — CURRENT SCANLINE IN VIDEO BLANKING INTERVAL ?   NO

525 — SWAP READY PIN LOGICALLY TRUE ?   NO

530 — SCAN OUT DATA AT VIDEO START ADDRESS

535 — RESUME RENDERING

END

FIG. 5B

550

START

555 — RECEIVE FRAME DIVIDER

560 — SUSPEND RENDERING

565 — SCANLINE IN VIDEO BLANKING INTERVAL ?   NO

570 — SWAP READY PIN LOGICALLY TRUE ?   NO

575 — PERFORM SERIES OF BLOCK TRANSFER OPERATIONS TO PERFORM BUFFER SWAP

580 — RESUME RENDERING

END

CONTROL
FLOW
— 600

698

(PORT DETECTED)

601

TEST FOR SYNC
CONNECTION

602

SYNC
CONNECT ? — YES

NO

603

DO NOT
ACTIVATE PORT/
DISPLAY
WARNING

604

CHECK FOR
SYNC OPTIONS

605

TEST SYNC AND
CONNECTION
STATUS

606

DESKTOP
OVERLAP
ON ? — NO

YES

607

SET AND READ
HORIZONTAL
AND VERTICAL
OVERLAP SIZES

608

BLENDING
ON ? — NO

YES

609

SET AND READ
HORIZONTAL
AND VERTICAL
BLENDING SIZES

610

SET AND READ
HORIZONTAL
AND VERTICAL
ROLL - OFF
INTENSITY

611

SET AND READ
HORIZONTAL
AND VERTICAL
LUMA

699 — (RETURN)

FIG. 6A

ATTY DKT. NO.: NVDA/P000876
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FILED: HEREWITH
APPLICANT: NVIDIA Corporation
TITLE: METHOD FOR TESTING SYNCHRONIZATION AND CONNECTION
STATUS OF A GRAPHICS PROCESSING UNIT MODULE
INVENTOR: IAN M. WILLIAMS, ET AL.
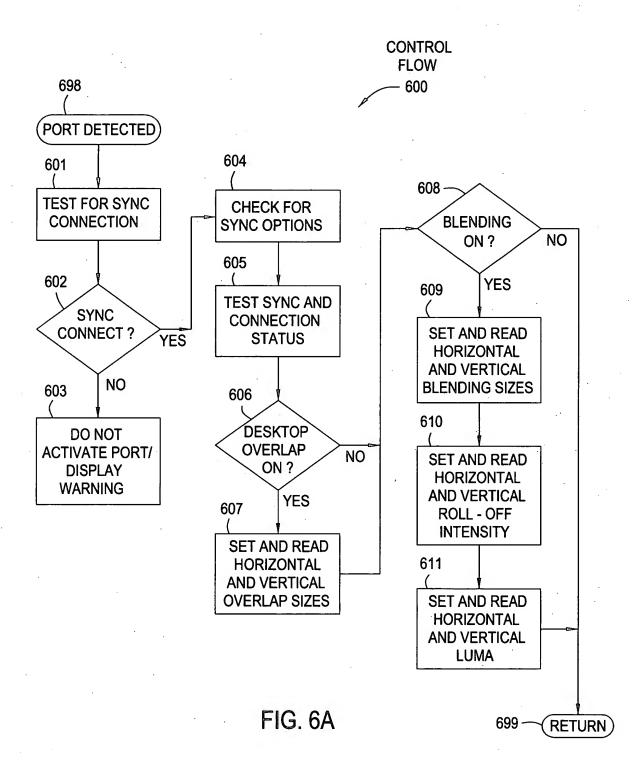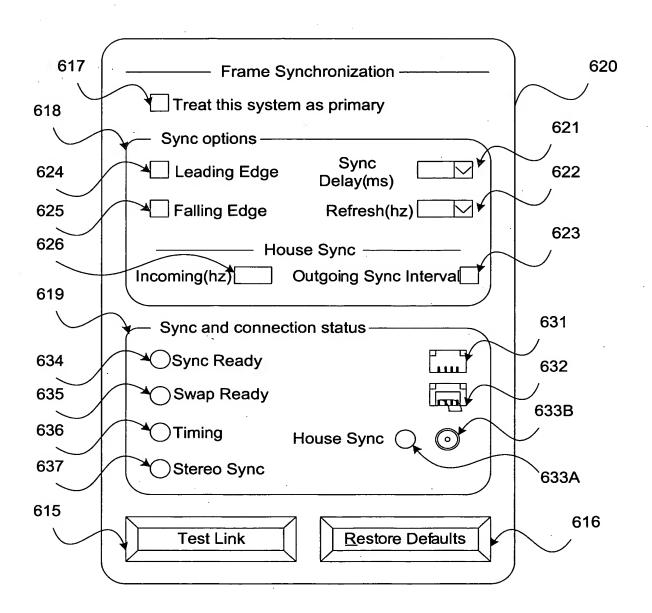EXPRESS MAIL NO.: EV335471017US   PAGE 18 OF 27

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617
620

Frame Synchronization

618 □ Treat this system as primary

Sync options

621

624 □ Leading Edge   Sync
Delay(ms)

622

625 □ Falling Edge   Refresh(hz)

623

626   House Sync

Incoming(hz)   Outgoing Sync Interval

619

Sync and connection status

631

634 ◯ Sync Ready

632

635 ◯ Swap Ready

633B

636 ◯ Timing   House Sync ◯ ◉

637 ◯ Stereo Sync

633A

615

616

Test Link   Restore Defaults

FIG. 6B

ATTY DKT. NO.: NVDA/P000876
U.S. SERIAL NO.: UNKNOWN
FILED: HEREWITH
APPLICANT: NVIDIA CORPORATION
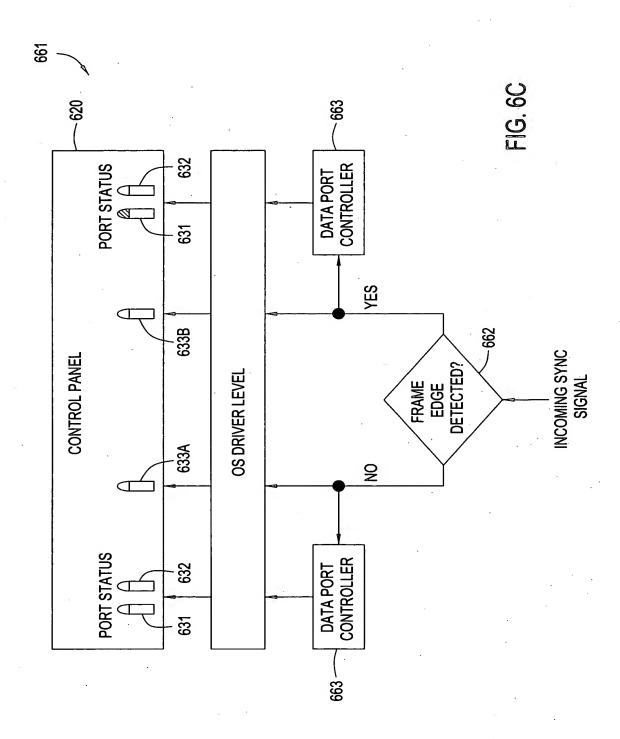TITLE: METHOD FOR TESTING SYNCHRONIZATION AND CONNECTION
STATUS OF A GRAPHICS PROCESSING UNIT MODULE
INVENTOR: IAN M. WILLIAMS, ET AL.
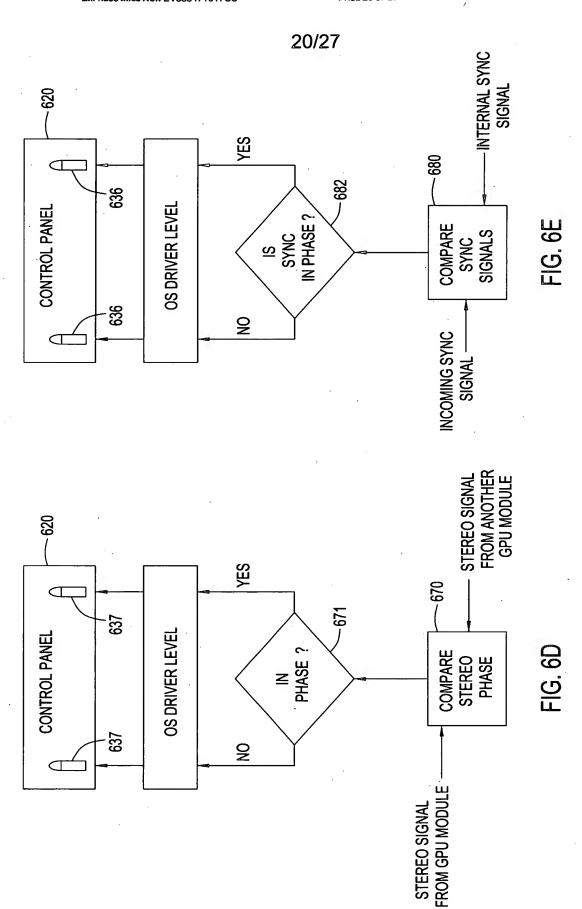EXPRESS MAIL NO.: EV335471017US   PAGE 19 OF 27

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FIG. 6C

FIG. 6E

FIG. 6D

ATTY DKT. NO.:   NVDA/P000876
U.S. SERIAL NO.:   UNKNOWN
FILED: HEREWITH
APPLICANT: NVIDIA CORPORATION
TITLE: METHOD FOR TESTING SYNCHRONIZATION AND CONNECTION
                    STATUS OF A GRAPHICS PROCESSING UNIT MODULE
INVENTOR: IAN M. WILLIAMS, ET AL.
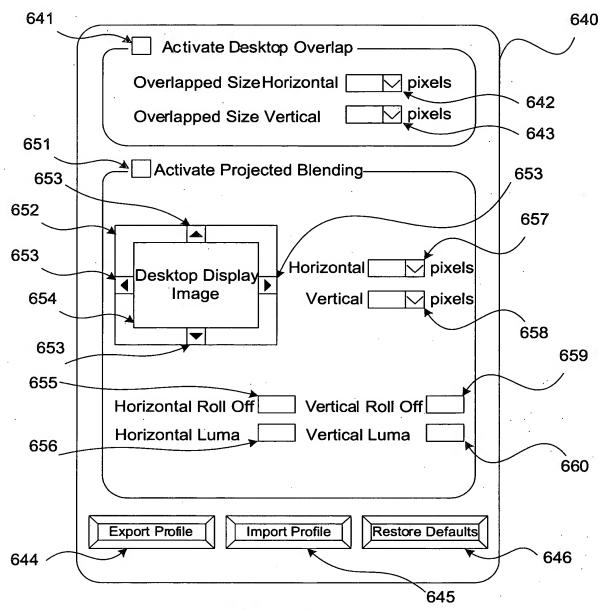EXPRESS MAIL NO.: EV335471017US   PAGE 21 OF 27

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FIG. 6F

ATTY DKT. NO.: NVDA/P000876
U.S. SERIAL NO.: UNKNOWN
FILED: HEREWITH
APPLICANT: NVIDIA Corporation
TITLE: METHOD FOR TESTING SYNCHRONIZATION AND CONNECTION
STATUS OF A GRAPHICS PROCESSING UNIT MODULE
INVENTOR: IAN M. WILLIAMS, ET AL.
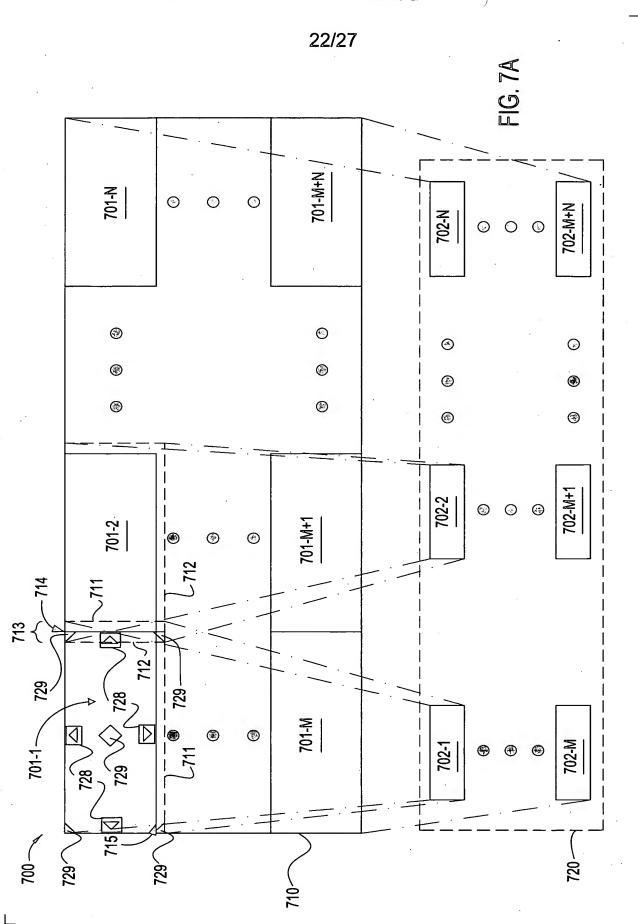EXPRESS MAIL NO.: EV335471017US   PAGE 22 OF 27

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FIG. 7A

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U.S. SERIAL NO.:   UNKNOWN
FILED: HEREWITH
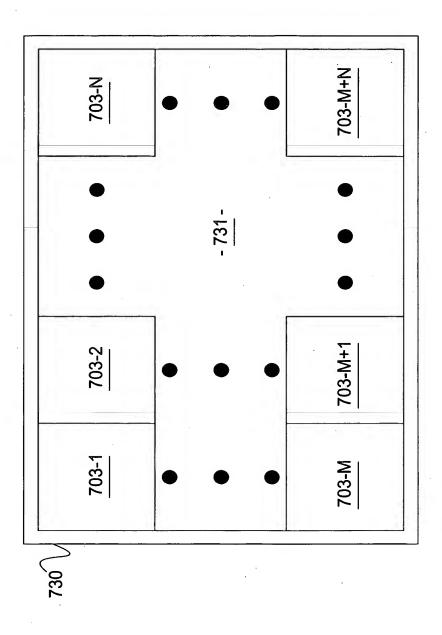APPLICANT: NVIDIA CORPORATION
TITLE: METHOD FOR TESTING SYNCHRONIZATION AND CONNECTION
                     STATUS OF A GRAPHICS PROCESSING UNIT MODULE
INVENTOR: IAN M. WILLIAMS, ET AL.
EXPRESS MAIL NO.: EV335471017US   PAGE 23 OF 27

FIG. 7B

ATTY DKT. NO.:   NVDA/P000876
U.S. SERIAL NO.:   UNKNOWN
FILED: HEREWITH
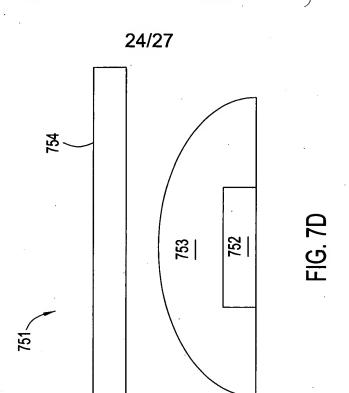APPLICANT: NVIDIA Corporation
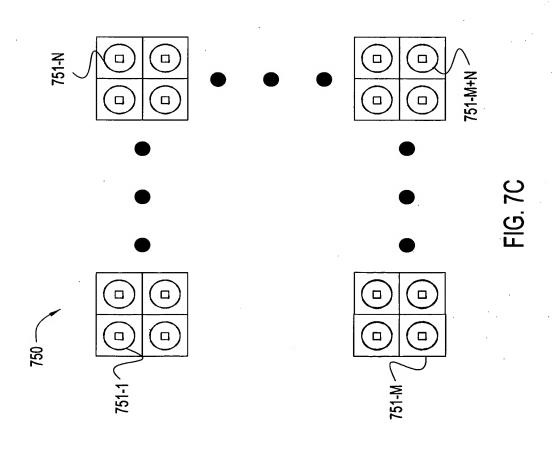TITLE: METHOD FOR TESTING SYNCHRONIZATION AND CONNECTION
                   STATUS OF A GRAPHICS PROCESSING UNIT MODULE
INVENTOR: IAN M. WILLIAMS, ET AL.
EXPRESS MAIL NO.: EV335471017US   PAGE 24 OF 27

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FIG. 7D

FIG. 7C

ATTY DKT. NO.: NVDA/P000876
U.S. SERIAL NO.: UNKNOWN
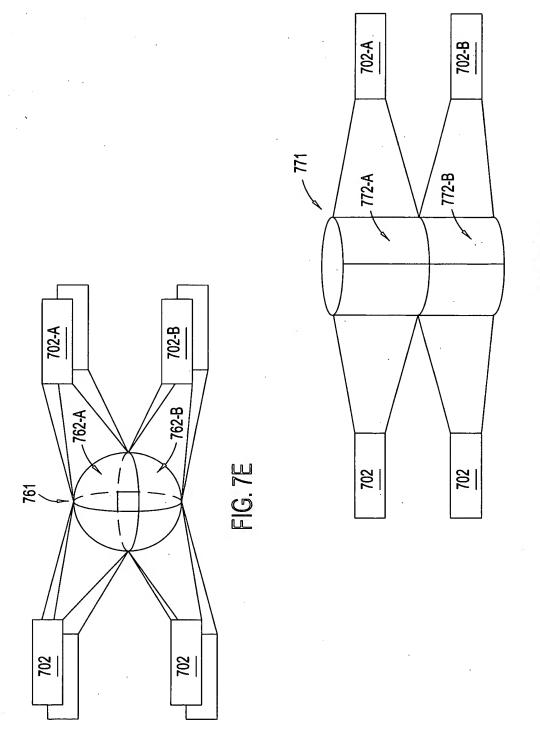FILED: HEREWITH
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TITLE: METHOD FOR TESTING SYNCHRONIZATION AND CONNECTION
STATUS OF A GRAPHICS PROCESSING UNIT MODULE
INVENTOR: IAN M. WILLIAMS, ET AL.
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FIG. 7E

FIG. 7F

ATTY DKT. NO.: NVDA/P000876
U.S. SERIAL NO.: UNKNOWN
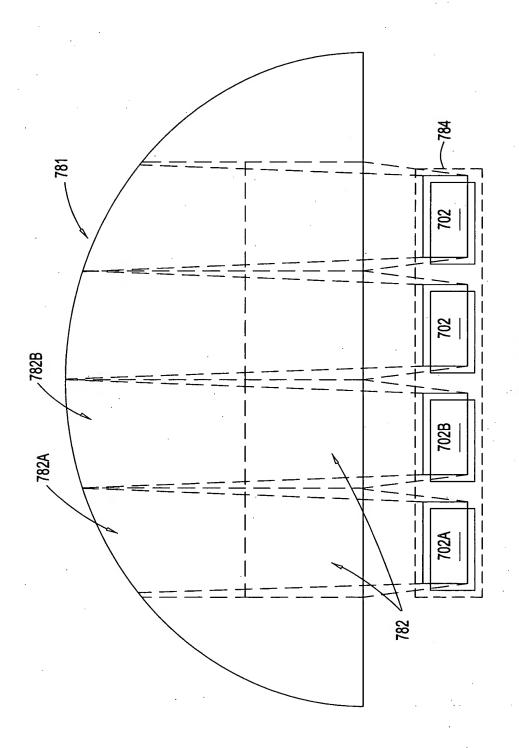FILED: HEREWITH
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TITLE: METHOD FOR TESTING SYNCHRONIZATION AND CONNECTION
STATUS OF A GRAPHICS PROCESSING UNIT MODULE
INVENTOR: IAN M. WILLIAMS, ET AL.
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FIG. 7G

ATTY DKT. NO.:   NVDA/P000876
U.S. SERIAL NO.:   UNKNOWN
FILED: HEREWITH
APPLICANT: NVIDIA CORPORATION
TITLE: METHOD FOR TESTING SYNCHRONIZATION AND CONNECTION
                   STATUS OF A GRAPHICS PROCESSING UNIT MODULE
INVENTOR: IAN M. WILLIAMS, ET AL.
EXPRESS MAIL NO.: EV335471017US   PAGE 27 OF 27

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FIG. 7J

FIG. 7H

FIG. 7I